Resistorless BJT bias and curvature compensation circuit at 3.4 nW for CMOS bandgap voltage references

O. E. Mattia, H. Klimach and S. Bampi

A novel resistorless bipolar junction transistor (BJT) bias and curvature compensation circuit for ultra-low power CMOS bandgap voltage references (BGR) is introduced. It works in the nano-ampere current consumption range and under 1 V of power supply. The analytical behavior of the circuit is described, and simulation results for a 0.18-µm CMOS standard process are analysed. A junction voltage of 550 mV at room temperature is obtained (at an emitter current of 3.5 nA), presenting an almost linear temperature dependence, while the power consumption of the whole circuit is 3.4 nW under a 0.8 V power supply at 27 °C. The estimated silicon area is 0.00135 mm².

Introduction: Voltage references are fundamental circuit blocks, ubiquitously used in analog, mixed-signal, RF and digital systems, including memories. The importance of low power design is self-evident in mobile and energy harvesting applications, while resistorless approaches enable the implementation of the circuit in standard digital processes.

Basically, the bandgap voltage reference, introduced by Widlar in 1971 [1], can be divided into three fundamental functions: the generation of two voltages or currents, one proportional and the other complementary to absolute temperature (PTAT and CTAT, respectively), and biasing. The biasing function sometimes is implemented inside the PTAT generator, reducing area and complexity, as is done in the traditional BGR approach [1]. In recent resistorless [2] and low-power [3] references, dedicated biasing blocks were used, increasing complexity, area and power consumption.

While in most cases the PTAT voltage source is inherently linear (proportional to the thermal potential φt), the CTAT voltage is traditionally implemented with a p-n junction, that has a slightly non-linear behavior over temperature [4]. This non-linearity is the main contributor to the temperature usually seen in BGR circuits, which directly impacts the thermal coefficient of the reference. Through the years, many curvature compensation techniques were proposed, but in general they need resistors and are somewhat complex [5].

In this Letter we propose a new self-biased CTAT circuit, where the BJT junction voltage is counterbalanced by the MOSFETs’ gate-source voltages, without the need for resistors, resulting in a very simple and small area topology. It works in the nano-ampere current consumption range and under 1 V of power supply. Also, the temperature curvature of the junction voltage can be controlled independently of the chosen bias point, as will be shown in the following section.

Circuit Description: The basic concept of our topology is shown in Fig. 1. In this circuit, the BJT junction voltage is counterbalanced by the gate-source voltage of N stacked nMOS transistors. The resulting VC2+3 defines the BJT bias current, through a feedback path that uses a current mirror with gain K. By defining N and K, a non-zero equilibrium DC point can be reached, which reflects the current-voltage behaviour of both the BJT and the MOSFETs.

\[ I_E = I_{SE} \exp \left( \frac{V_{BE}}{m \phi_t} \right) \]  (1)

Where \( V_{BE} \) is the emitter-base voltage, m represents the slope factor and \( I_{SE} \) is the reverse saturation current for the p-n junction. Assuming that all MOSFETs are operating in subthreshold regime and saturated (\( V_{DS} \geq 100 \) mV), the drain current \( I_D \), according to the ACM MOSFET model [6], is given by (2).

\[ I_D = 2 I_{SQ} \frac{W}{L} \exp \left( \frac{V_G - V_{TH}}{m \phi_t} - \frac{V_S}{\phi_t} \right) \]  (2)

\( I_{SQ} \) is the specific current per square, which is a process dependent parameter defined by carrier mobility, oxide capacitance and temperature. \( V_{TH} \) is the threshold voltage for zero bulk-source voltage, and \( V_G \) and \( V_S \) are the gate and source voltages referred to the substrate, respectively. Assuming that all MOSFETs have the same width \( W \) and length \( L \), and present the same slope factor \( n \) (since the bulk-source voltage is zero), leads to \( I_{SE} = V_E/N \). Substituting (1) and (2) into the equality \( K_1 I_D = I_E \), and solving for the junction voltage \( V_E \), leads to (3).

\[ V_E = \frac{\phi_t}{(2 + 2 n) \ln \left( 2k W I_{SQ} L I_{SE} \right)} V_{TH} - \frac{V_{TH}}{m \phi_t} \]  (3)

By changing the number of series nMOS transistors and the constant gain, different derivatives of \( \Delta V_E/\Delta T \) can be generated. In Fig. 2a we present the junction voltage behavior, and its first derivative on Fig. 2b, for five different bias circuits: (i) an ideal constant current source (Idc); (ii) a PTAT current source as generated in the traditional BGR (Iptat); (iii) the concept circuit with \( K_1 = 1 \) and \( N_2 = 2 \) (12M); (iv) the concept circuit with \( K = 19.63 \) and \( N = 3 \) (13M); and (v) the concept circuit with two nMOS branches adding their currents into the BJT emitter, as shown in Fig. 3, being \( K_1 = 1 \), \( N_1 = 2 \), \( K_2 = 1.2 \) and \( N_2 = 3 \) (I2+3M). All circuits were designed to provide the same junction voltage of 550 mV at 27 °C.

\[ \frac{\partial V_E}{\partial T} \]  (4)

As a metric of linearity, we can use the total variation of the first derivative \( V_E \), \( \Delta (\partial V_E/\partial T) \), and the average of the second derivative \( \partial^2 V_E/\partial T^2 \) for both conditions: (i) the proposed circuit (I2+3M) in a weighted way results in an improvement in linearity, as shown in Fig. 2c. This happens because the branch with three nMOSFETs, shown in Fig. 3, will increase the junction current at higher temperatures, decreasing its voltage derivative.

Simulation Results: The proposed circuit implementation (I2+3M) is presented in Fig. 3, where two MOSFET branches using \( N_1 = 2 \) and \( N_2 = 3 \) are used to bias the BJT. The current mirroring factors \( K_1 \) and \( K_2 \) were adjusted to obtain the lowest curvature of the thermal dependency of \( V_E \), for the condition \( V_E = 550 \) mV at \( T = 27 \) °C. This bias voltage was chosen because of the low current consumption of the BJT (\( I_E = 3.5 \) nA).

The proposed topology can also be implemented without floating-well nMOSFETs, which means that simpler and cheaper processes can be used. In this case, the \( V_E \) voltage is not equally divided between the stacked nMOSFETs, because of the body effect that increases the threshold voltage on the devices with \( V_G > 0 \). Practically, this reduces the drain current of the MOS branches and can be compensated by increasing the current gains \( K_1 \) and \( K_2 \). In Fig. 4a, we present the \( V_E \) results for both conditions: (i)

\[ I_E = I_{SE} \exp \left( \frac{V_{BE}}{m \phi_t} \right) \]  (1)

\[ I_D = 2 I_{SQ} \frac{W}{L} \exp \left( \frac{V_G - V_{TH}}{m \phi_t} - \frac{V_S}{\phi_t} \right) \]  (2)

\[ V_E = \frac{\phi_t}{(2 + 2 n) \ln \left( 2k W I_{SQ} L I_{SE} \right)} \left[ \ln \left( 2k W I_{SQ} L I_{SE} \right) \right] - \frac{V_{TH}}{m \phi_t} \]  (3)

Fig. 1. Schematic of the bias circuit concept.

The emitter current \( I_E \) of the bipolar transistor is given by (1).
sensitivity is 244.6 pA/V and 204.1 pA/V - Fig. 5

with a line sensitivity of 1.3 mV/V for both. The current consumption have the same channel length

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estimated silicon area of 0.00135 mm\(^2\).

power consumption of 3.4 nW, under a 0.8 V power supply, with an estimated silicon area of 0.00135 mm\(^2\).

Conclusion: A novel resistorless BJT bias topology was presented, with main application in low-power bandgap voltage references. It is composed by MOSFETs in subthreshold and a vertical parasitic PNP BJT only, and implements curvature compensation independently of the bias voltage chosen. The topology was simulated in a 0.18\(\mu\)m CMOS technology, resulting in a junction voltage at room temperature of 550 mV, with a power consumption of 3.4 nW, under a 0.8 V power supply, with an estimated silicon area of 0.00135 mm\(^2\).

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References


3 Osaki, Y. et al.: ‘1.2-V Supply, 100-nW, 1.09-V Bandgap and 0.7-V Supply, 52.5-nW, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS LSIs’, *IEEE J. Solid-State Circuits*, 2013, 48, (6), pp. 1530-1538


Fig. 3. Schematic of proposed bias and curvature compensation circuit.

Fig. 4 (Fig. 4a) junction voltage \(V_{JE}\); (Fig. 4b) \(V_E\) first derivative; and (Fig. 4c) total current consumption over temperature, for the circuit of Fig. 3.

Referring to Fig. 4, \(\Delta(\partial V_E/\partial T) = 66.81 \mu\)V/\(\circ\)C for the floating-well circuit, while the grounded-well achieved \(\Delta(\partial V_E/\partial T) = 56 \mu\)V/\(\circ\)C. As a comparison, the PTAT current biasing shown in Fig. 2 achieves \(\Delta(\partial V_E/\partial T) = 78.41 \mu\)V/\(\circ\)C, and the constant current biasing achieves \(\Delta(\partial V_E/\partial T) = 127 \mu\)V/\(\circ\)C, demonstrating the improvement of the proposed topology. The current consumption at 27 \(\circ\)C for the whole circuit is 6.49 nA and 4.3 nA, reaching a maximum of 14.27 nA and 16.46 nA at 125 \(\circ\)C, for the floating-well and the grounded-well nMOSFET circuits, respectively. Both circuits were designed to achieve similar maximum power consumptions. In the case of the grounded-well nMOSFETs, the three stacked transistor branch contributes more to the bias current, and that explains why there are differences in \(\partial V_E/\partial T\) and in the total current.

Even though the nominal supply voltage of the process used is 1.8 V, both implementations start operating around 0.7 V, as shown in Fig. 5a, with a line sensitivity of 1.3 mV/V for both. The current consumption sensitivity is 244.6 pA/V and 204.1 pA/V - Fig. 5b, again for the floating-well and grounded-well nMOSFET circuits, respectively. Power supply rejection ratio (PSRR), measured at 100 Hz and \(V_{DD} = 0.8\) V, is around -50 dB - Fig. 5c for both implementations, even though the grounded-well circuit has a lower PSRR at higher frequencies, since its body is attached directly to the ground line. PSRR could be increased by adding cascode current sources, at the penalty of increasing the minimum supply voltage. The estimated silicon area for the grounded-well circuit is 0.00135 mm\(^2\).

Fig. 5 (Fig. 5a) Junction voltage; and (Fig. 5b) total current versus power supply; (Fig. 5c) PSRR versus frequency.

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